Roll No.

CONTROLLER OF EXAMINATIONS ★ ADDITIONAL AU CHENNAI 600 025

ANNA UNIVERSITY (UNIVERSITY DEPARTMENTS)
B.Tech IT (Full Time) - END SEMESTER EXAMINATIONS, MAY 2025
III Semester
IT5301 - DIGITAL LOGIC DESIGN
(Regulation2019)

Time:3hrs Max.Marks: 100

CO1	Simplify complex Boolean functions.
CO2	Implement digital circuits using combinational logic ICs and PLDs.
CO3	Understand the characteristics of various Flip-Flops.
CO4	Design digital circuits with combinational and sequential components
CO5	Use HDL to build digital systems
CO6	Analyze digital system designs

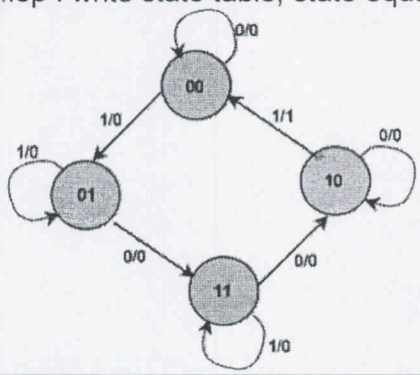
BL – Bloom's Taxonomy Levels
(L1-Remembering, L2-Understanding, L3-Applying, L4-Analysing, L5-Evaluating, L6-Creating)

PART- A(10x2=20Marks)
(Answer all Questions)

Q.No	Questions	Marks	CO	BL
1	Simplify using Boolean laws and Theorem :- (P'+R')(P+R+Q'S)	2	CO1	L2
2	Perform binary subtraction using 2s complement method for the decimals (13-17)	2	CO2	L2
3	Express the minterm of the function x'y'+xz'	2	CO1	L2
4	Write an HDL code for implementing half Adder	2	CO5	L1
5	Design a 2X4 decoder circuit.	2	CO4	L3
6	Write (1101)2 equivalent code in GREY and BCD codes	2	CO2	L1
7	Write characteristic table and equation of JK flipflop	2	CO3	L2
8	Design a two bit down counter using negative edge T FF	2	CO4	L3
9	Compare simple and complex PLDs	2	CO6	L2
10	Implement a Half adder using PLA	2	CO2	L3

PART- B(5x 13=65Marks)

Q.No	Questions	Marks	CO	BL
11 (a) (i)	Express the following function as SOP and POS f = xz' + xy'z + w'z' + wx'yz' Give truth table Draw logic circuit using primitive gates. Draw logic circuit using nor gates only	4 3 3 3	CO1	L3
OR				
11 (b) (i)	List atleast 10 Boolean laws and theorem and write the proof for the DeMorgan's Theorem.	13	CO1	L2
12 (a) (i)	Design a full Adder and write the HDL code for the same circuit. Also extend the full adder to implement n bit addition	13	CO4 & CO5	L3
OR				
12 (b) (i)	Using of K maps, find the simplest sums of product form of the function F(W,X,Y,Z) = Σ (0,1,3,6,9,10,14) + d(8, 13). Draw the logic circuit using primitive gates and also using NAND only	13	CO4	L3

13 (a) (i)	Design and Implement a BCD to Grey code convertor using primitive gates.	**13**	CO4	L3
OR				
13 (b) (i)	Design a two bit comparator circuit and also logically extend it for implementing n bit comparison	**13**	CO2	L3
14 (a) (i)	Design a synchronous counter using T flip-flop with the following sequence 0000 >0010 >0100 >0111 >1001 >000	**13**	CO4	L3
OR				
14 (b) (i)	Design a sequential circuit for the given state diagram using JK flipflop . write state table, state equation and draw circuit diagram  	**13**	CO4	L3
15 (a) (i)	Draw the logical construction of a 4 X 4 RAM incorporating the binary cell with various input and output pins	**4**	CO2	L2
(ii)	Tabulate the PLA programming table and implement the three boolean functions such that you minimize the number of product terms to deploy the circuit. $A(X,Y,Z) = \Sigma (1,3,4,5)$ $B(X,Y,Z) = \Sigma (0,1,2,6,7)$ $C(X,Y,Z) = \Sigma (2,3,6,7)$	**9**	CO2	L3
OR				
15 (b) (i)	Discuss about FPGAs.	**4**	CO2	L2
(ii)	Tabulate the PAL programming table and implement the three boolean functions such that you minimize the number of product terms to deploy the circuit. $A(X,Y,Z) = \Sigma (1,2,3,4,5)$ $B(X,Y,Z) = \Sigma (0,1,2,3,6,)$ $C(X,Y,Z) = \Sigma (2,4,5,6).$	**9**	CO2	L3

PART- C(1x 15=15Marks)

Q.No	Questions	Marks	CO	BL
16.	Design and develop a digital system to monitor a lift (elevator) in a multistorey building. The building has 100 floors. Count the number of times a floor with Fibonacci number is selected and also a blue led glows whenever the lift stops at the Fibonacci floor. An alarm is raised if the lift is toggling between any two floors more than 10 times continuously. To implement the system, use appropriate combinational and sequential blocks of circuit working ina integrated fashion. Design the system Draw block diagram Draw logic diagram for each block Write HDL code for virtually simulating this system	**15**	CO4	L4